REMARKS

By the foregoing amendments, claims 2, 6, 8, 18, 20 and 23 have been cancelled and claims 1, 3-5, 11, 13, 19, 21, 22, 25 and 26 have been amended. Thus, claims 1, 3-5, 7, 9-17, 19, 21, 22 and 24-26 remain in the application.

Claims 7, 8, 18 and 23 were rejected in the outstanding Office Action under 35 U.S.C. §112, second paragraph, as being indefinite because allegedly it is unclear as to what is the exact adhesive strength. Responsive to this rejection, the application claims have been amended or cancelled so as to delete reference to adhesive strength. In view of these changes, it is respectfully submitted that the claims as amended are proper under 35 U.S.C. §112, second paragraph.

Claims 1-5 stand rejected in the Office Action under 35 U.S.C. §102(b) as being anticipated by the patent to Milewski, U.S. Patent No. 6,330,967 as stated on pages 2 and 3 of the Office Action. In this regard it is noted that the patent number for the patent to Milewski is misstated in paragraph number 5 on page 2 of the Office Action. This rejection is hereby traversed and reconsideration thereof is respectfully requested in view of the above amendments to the claims and Applicants remarks set forth below.

The patent to Milewski et al. discloses a process to produce a high temperature interconnection. The reference is relied upon for its disclosure in Figure 5A wherein a die 10 is joined to a substrate 21 by a lead-tin eutectic alloy solder 39 which is formed by melting a low melting point cap 37 of tin on a high melting point ball 35 of lead to form the eutectic lead-tin alloy 39. Thereafter, the assembly is annealed several hours at a temperature below

the melting point of the eutectic alloy to cause tin from the eutectic alloy to diffuse into the lead-rich ball 35 and thereby raise the melting point of the alloy 39. The assembly 33 formed by the high melting point ball 35 of lead and the low melting point cap 37 of tin, as shown in Figure 4 of the patent drawings, is a nonreflowed solder assembly. Moreover, this assembly is joined to a conventional recessed land 51 on substrate 21. The recessed land 51 can be formed of copper. The thin, recessed pads 51 are solder wettable I/O terminals or adhesion pads and not standoffs which extend above the substrate in the form of a stiff bump. The high melting point ball 35 is also not reflowed during the joining process, which takes place at a temperature below the melting point of the lead ball.

In contrast, the electronic assembly of the present invention as recited in claim 1 as amended comprises a substrate, a die, and a plurality of interconnections between the substrate and die, wherein respective ones of the interconnections include a relatively low melting temperature and yield strength reflowed solder bump on the die, a relatively higher melting temperature and electrically conductive material standoff on the substrate in the form of a stiff bump extending above the substrate surface and having a yield strength in the 350-450 MPa range, and a soldered joint connecting the reflowed solder bump to the electrically conductive material standoff.

Applicants' invention considers and solves the problem of thin film, interlayer dielectric (ILD) delamination under the die bumps during temperature cycling of the package by lowering the yield strength of the die bump material in relation to the copper standoff on the substrate. The patent to Milewski et al. does not relate to an electronic assembly having a copper

bump standoff, a stiff structure as compared with the thin copper pad of the reference as noted above. Moreover, the solder bump assembly 33 in Milewski et al. is a nonreflowed solder assembly. The high melting point ball 35 of the assembly is not reflowed during soldering of the die and substrate to one another as is the solder bump of the present invention.

Thus, the electronic assembly of Milewski et al. is different than that of the present invention. Milewski et al. recognize the problem of delamination as noted in column 2, lines 38-41, but suggest a different solution to the problem than that of the present invention. The solution by Milewski et al. is not one wherein the electronic assembly includes a standoff in the form of a stiff bump extending above the substrate surface and having a yield strength in the 350-450 MPa range as does the copper standoff in the example embodiment of the present invention as disclosed in Applicants' specification.

In view of the above amendments and remarks, it is respectfully submitted that Applicants claims as amended are not anticipated, 35 U.S.C. §102, are rendered obvious, 35 U.S.C. §103, in view of the patent to Milewski et al.

Claims 1, 6, 7, 19-22, 25 and 26 were rejected in the Office Action under 35 U.S.C. §102(b) as being anticipated by Yamamoto (JP10-12659) as stated on pages 3 and 4 of the Office Action. Claims 9-17 and 24 have been rejected under 35 U.S.C. §103(a) as being unpatentable over Yamamoto in combination with Dalal (JP08-332590). The references were combined in the rejection for the reasons and in the manner stated on pages 4 and 5 of the Office Action. These rejections are hereby traversed and reconsideration

thereof is respectfully requested in view of the above amendments to the claims and Applicants remarks set forth below.

The reference to Yamamoto discloses a connection structure of an electronic component wherein the die, 21 in Figure 8, has a metallic bump of copper thereon like the prior art connection structure depicted in Figures 1-3 of the application drawings. The present invention is an improvement over such a prior art connection structure in that an electrically conductive material standoff in the form of a stiff bump is provided on the substrate so as to extend above the substrate surface, the standoff having a yield strength in the 350-450 MPa range. Whereas the die, on the other hand has a relatively low melting temperature and yield strength reflowed solder bump thereon which is soldered to the standoff. It has been found that this electronic assembly, semiconductor package and method of interconnecting a die and substrate to one another of the invention result in reduced die stresses for avoiding ILD delamination as discussed in Applicants specification.

Independent claims 1, 11, and 19 which stand rejected based on the patent to Yamamoto, either taken alone or in combination with the Dalal reference, have been amended to clarify the aforementioned differences between the present invention and the connection structure of Yamamoto. The die in Yamamoto does not include a reflowed solder bump with a relatively lower yield strength which is soldered to a standoff contact member on the substrate as in the present invention. Rather, the die 21 of Yamamoto is provided with the conventional copper metallic bump 28, like the prior art of Applicants' Figures 1-3, which is joined by a thin solder layer 29 to a solder bump 36 on substrate 21. The problem of high peeling stress on the ILD

material with such a construction, particularly at the edge of the copper bump on the die, is discussed in connection with Applicants' Figures 5-7 of the application drawings. The present invention avoids or reduces this problem as discussed in the application.

The secondary reference to Dalal, JP08-332590, was cited for its disclosure of using a ceramic substrate having a thermal expansion of 15ppm-°C. Admittedly, materials having a such a thermal expansion are, per se, known. However, Applicants' electronic assembly, semiconductor package and method of interconnecting a die and a substrate as recited in Applicants' claims are not disclosed or rendered obvious by the secondary reference, either taken alone or in combination of Yamamoto.

In view of the above amendments and remarks, it is respectfully submitted that the application claims as amended now patentably define over the cited references. Accordingly, reconsideration and allowance of the claims as amended are respectfully requested.

Attached hereto is a marked-up version of the changes made to the claims by the current amendment. The attached page is captioned **"Version with markings to show changes made."**

To the extent necessary, Applicants petition for an extension of time under 37 CFR §1.136. Please charge any shortage in the fees due in connection with the filing of this paper, including extension of time fees, to

Deposit Account No. 01-2135 (Case No. 219.40780X00) and please credit any excess fees to such deposit account.

Respectfully submitted,

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VERSION WITH MARKINGS TO SHOW CHANGES MADE

IN THE CLAIMS:

Please cancel claims 2, 6, 8, 18, 20 and 23 and amend the claims to read as follows:

1. (Amended) An electronic assembly comprising:

a substrate;

a die;

a plurality of interconnections between the substrate and die;

wherein respective ones of the interconnections include a relatively low melting temperature and yield strength reflowed solder bump on the die, a relatively higher melting temperature and electrically conductive material standoff on the substrate in the form of a stiff bump extending above the substrate surface and having a yield strength in the 350-450 MPa range, and a soldered joint connecting the reflowed solder bump to the electrically conductive material standoff.

3. (Amended) The electronic assembly according to claim [2] 1, wherein the top surface of the standoff is wetted by the reflowed solder bump to form the soldered joint.

4. (Amended) The electronic assembly according to claim [2] 1, wherein the standoff is a bump in the form of a column or stud.

5. (Amended) The electronic assembly according to claim 1, wherein the relatively higher melting temperature and electrically conductive material standoff is copper.

11. (Amended) A semiconductor package comprising:

a package substrate having a coefficient of thermal expansion of at least 15 ppm/°C, the package substrate having a plurality of relatively high melting temperature and electrically conductive standoff contact members on the substrate;

a die having a coefficient of thermal expansion which is at least 2.7 ppm/°C less than that of the substrate, a front side of the die having a plurality of relatively lower yield strength reflowed solder [connections] bumps thereon, the die being located on the substrate with the solder [connections] bumps connected to the respective ones of the standoff contact members by soldered joints electrically coupling the die to the substrate.

13. (Amended) The semiconductor package according to claim 12, wherein the standoff contact members comprise a plurality of standoff elements upstanding from a surface of the substrate, and wherein the soldered joints connect the [semiconductor chip] die to the tops of respective ones of the standoff elements.

19. (Amended) A method of interconnecting a die and substrate to one another for reduced die stresses, the method comprising:

providing a relatively low melting temperature and yield strength solder bump on a die and a relatively higher melting temperature and electrically conductive material standoff contact member on a substrate; and

[forming] reflow soldering the solder bump to form a soldered joint connecting the solder bump to the electrically conductive material standoff contact member.

21. (Amended) The method according to claim [20] 19, wherein the solder bump is wetted on the top surface of the standoff contact member to form the soldered joint.

22. (Amended) The method according to claim 19, wherein the solder bump is provided over an inter layer dielectric material in the die.

25. (Amended) The method according to claim 19, wherein the reflow soldering includes separately heating the die and solder bump to at least a soldering temperature and thereafter contacting the solder bump with the standoff contact member on the substrate for forming the soldered joint.

26. (Amended) The method according to claim 25, further comprising separately heating the substrate to a temperature substantially lower than the reflow soldering temperature before contacting the solder bump on the die with the standoff contact member on the substrate to form the soldered joint.